© IJCIRAS | ISSN (O) - 2581-5334
October 2019 | Vol. 2 Issue. 5

ANALYSIS OF SINGLE-PHASE SIX-SWITCH DUAL-OUTPUT INVERTER

Kanchana Keshav Patgar[1], Mrs. Hemavathi. R[2]

[1]Student, UVCE, Bangalore and 560001, India
[2]Assistant Professor, UVCE, Bangalore and 560001, India

Abstract

Single-phase six switch dual-output inverter uses the two three-switch-leg structures. New topology of three-switch-leg is used for the dual output inverter. It has the benefits like improved reliability, absence of short circuit problems and higher efficiency. The active switches used in the circuit is MOSFET which has no issue of reverse recovery problems by its body diodes. Passive components also reduced be using high switching frequency of 30kHz. The circuit is built for input voltage of 12V DC and tested for resistive load. Three-level output voltage is obtained. The two-output obtained are for CF (common frequency) varies from 49.8Hz-50.2Hz. The efficiency of the circuit is calculated is to be 87.84%.

Keyword: dual-output, dual-buck inverter, reduced switch-count converter, single phase inverter, three-switch-leg

1.INTRODUCTION

Active switches like IGBT and MOSFET used in converters requires gate driver circuit and gate driver power supply. Which intern increases the cost of the circuit. And also, weight, volume of the circuit and probability of failure of the circuit also increases. Therefore, its important reduce the number of switches. For reducing switch count many topologies are introduced.

Switch count reduction in ac-dc-ac converter is achieved by well-known three methods. 1) split capacitor leg[2], 2) sharing phase leg[3], 3) three-switch-leg[4]. For this paper three-switch-leg method is used. Dual-output inverter are used in many applications like ac-ac nine switch converter, dual-output Z-source inverter, back-to-back converter for doubly fed induction generator, to drive six-phase motor, online uninterrupted power supply, multi input converter, energy system for distributed generation.

Fig1(a) represents the conventional circuit and its modulation scheme for the dual-output inverter. This circuit uses the topology three switch leg. In each leg it has three switches. Switches in the middle are common to both upper and lower outputs. To avoid short-circuit or open-terminal the upper reference should be always greater than the lower reference. Depending on the magnitude of the reference signal this circuit can be operated in two modes: common frequency (CF) and different frequency (DF) modes. In the CF mode, as the name indicates the fundamental frequencies output voltage of both the outputs are same. This is achieved by making magnitude of the reference signal to unity.

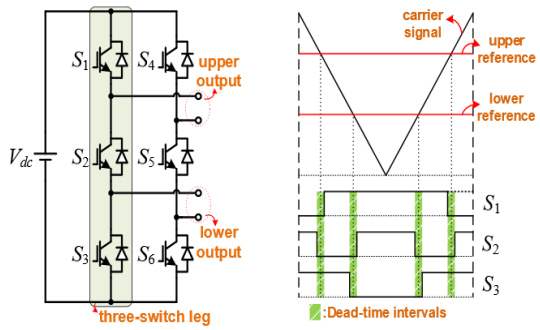

Figure 1(a) conventional dual-output six switch inverter (b) modulation scheme

Whereas, in the DF mode, two outputs of dual output inverter have a different fundamental frequency are different. This is achieved by making the magnitude of reference signal lowered to half or magnitude should be less than unity. In most of the application common frequency mode is used such as online-UPS or the same-speed drives system. Instead of using four-switch full-bridge, using three-switch-leg reduces 25 % of the

active semiconductor devices used in the system. But main problem in these circuit is short-circuiting when all switches in the phase leg being turned on simultaneously. Generally, a finite pulse-width modulation (PWM) dead time is used at the cost of a distorted output waveform and reduced achievable voltage gain.

Dual buck structure consists of two switches and a diode in the middle in one leg and two diode and one switch in the middle as shown in the fig.2. Two current limiting inductors L_p and L_n are used to limit the short through current. Short through current is nothing but current flowing in leg when all switches are simultaneously turned-on (over-lap time period). During this period current increases with slope $V_{dc}/2L_c$, where $L_c=L_p=L_n$. this provides time for the protection circuit to shut down.

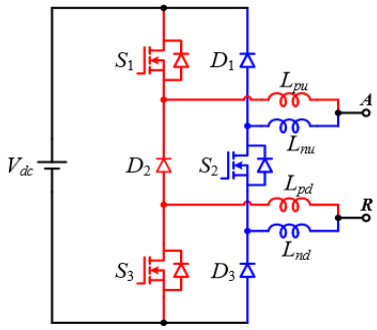

Figure 2 Three-switch-leg structure

Power MOSFETs are used as active switches. These MOSFETs has fast switching speed as compare to IGBTs. In MOSFETs lower switching and conduction losses due to resistive conduction voltage drop, as compare to IGBTs at a certain current level. The dual-buck leg has a unique structure, relieves the reverse recovery issues as body diodes of MOSFETs do not have a chance to conduct. Two externally selected fast recovery diodes (D_p and D_n) are used for freewheeling. Power MOSFETs can be used for higher switching frequency without severely compromising converter efficiency. Which intern leads to lesser filter requirement and avoids acoustic noise. Although two more current limiting inductors are required, the efficiency of the dual-buck leg can be higher than that of the IGBT based conventional leg.

2. OPERATION PRINCIPLE OF DUAL-BUCK THREE-SWITCH-LEG

The proposed leg operates in three switching states for switches [S1S2S3] as P [110], Z [101], and N [011] similar to conventional three-switch-leg. Where ic1 and ic2 represent the freewheeling of limiting inductor currents through the circuit loops if it occurs. Fig3(a),(b),(c). shows the these switching states. In these states' inductor voltage i.e. upper and lower inductor connected to P and N (L_{pu}, L_{nu}, L_{pd}, L_{nd}) are shown in the table1.

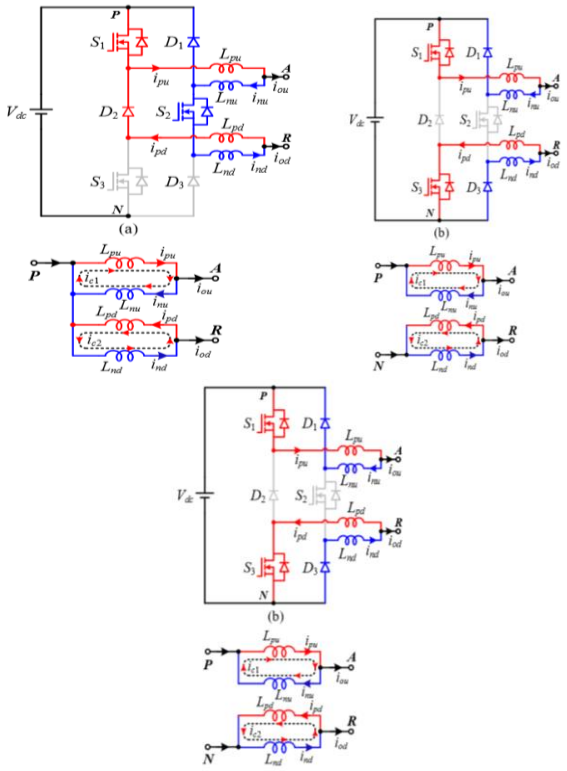

Figure 2 (a), (b), (c) switching states for Three-switch-leg P [110], Z [101], and N [011]

States	DEVICES						Inductor voltages	
	S1	D1	S2	D2	S3	D3	V_{Lpu},V_{Lnu}	V_{Lpd},V_{Lnd}
P[110]	On	Fb	On	Fb	Off	Rb	V_{PA}	V_{PR}
N[101]	On	Fb	Off	Rb	On	Fb		V_{NR}
Z[011]	Off	Rb	On	Fb	On	Fb	V_{NA}	

The limiting inductors used in dual buck structure. As the current through inductors will not change immediately depending on the inductor current path the circuit will have six modes in each switching states. Therefore, this

dual buck structure will have eighteen modes of operation.

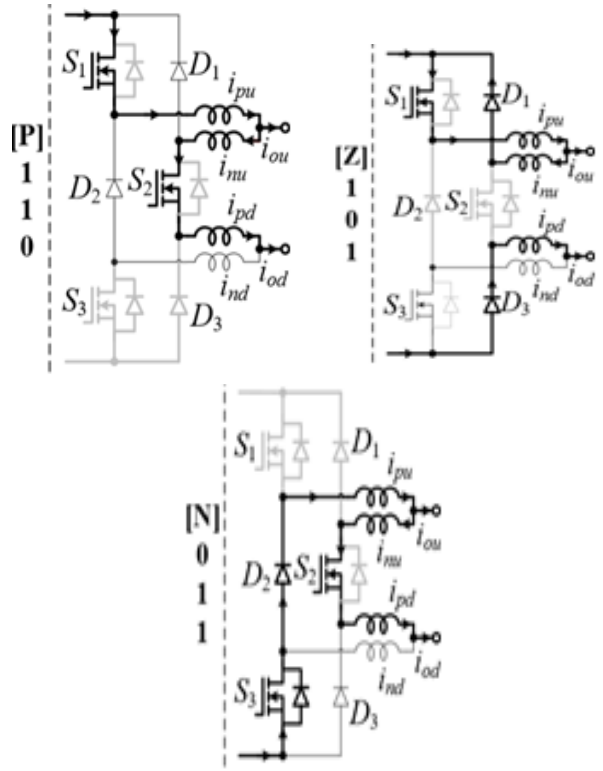

Figure 3 (a), (b), (c) different modes of operation of switching states for Three-switch-leg P [110], Z [101], and N [011]

Let's consider the switch is in 1st state i.e. P[110]. Switches S_1 and are turned on and diodes D_1 and D_2 are forward-biased the switch S_1 and inductor L_{pu} carries the total output currents (i_{ou} + i_{od}), whereas the switch S_2 and inductors L_{nu}, L_{pd} carries the lower output current (i_{od}). In this case, the inductor L_{nd} does not conduct any currents. Thus, the ic1 and ic2 are zero as shown in fig 3 (a) and current i_{ou} , i_{od} are greater than zero.

When switching state changes to Z[101] the current (i_{nu} = i_{od}) in L_{nu} freewheels through the loop of L_{nu}-D_1-S_1-L_{pu}. Thus, S_1 and L_{pu} still carries the total output currents (i_{ou} + i_{od}), the i_{c1} is i_{nu}. The lower output current (i_{od}) freewheels through D_3 and L_{pd} and the i_{c2} is zero as shown fig 3 (b).

Again changing the state from Z[101] to N[011], the current (i_{pu}=i_{ou}+i_{od}) in L_{pu} freewheel through S_3 and D_2. S_2, inductors L_{pd} and L_{nu} carries the lower output current as shown fig 3 (c). The circulating currents in inductors i_{c1} and i_{c2} are zero.

3. REVERSE RECOVERY PROBLEMS

In conventional dual-buck two-switch leg there is no issue of reverse recovery problem as the body diodes of MOSFETs do not have a chance to conduct because of the unidirectional currents in limiting inductors. But in the dual-buck three-switch-leg, the body diode of S_1 may conducts in three modes for the switching state P [110], the body diode of S_3 may conducts in 3 modes for the switching state N [011], In these cases, the reverse recovery process occurs as switches S_1 or S_3 is forced to be turned-off. the transition from P [110] or N [011] to Z [101], because of maintaining the switches S_1 and S_3 respectively being turned-on, no the reverse recovery problem in these transitions. When the switching state changes between P [110] and N [011], the S3 is first turned-off. Then, during dead-time, its body diode conducts the current. When the S_1 is turned-on, the body diode of S_3 is forced to turned-off and thus requires a reverse current to recombine the charge stored during its conduction time. Fortunately, during this transition, the diode D_2 are being forward-biased. Hence, it prevents occurring of the shoot-through. The reverse current should flow through the limiting inductors.

4. SINGLE PHASE SIX SWITCH DUAL OUTPUT INVERTER

single phase six switch inverter consists of two three switch leg as shown in fig 19. For each leg there is three switching states P [110], Z [101], and N [011]. And this single phase has two such three switch leg. These legs operate in combination of these tree switching states.

Therefore, this circuit has nine switching states like PP, ZZ, NN, PN, PZ, ZP, ZN, NP and NZ. Corresponding upper and lower output voltage voltages are given in the table2.

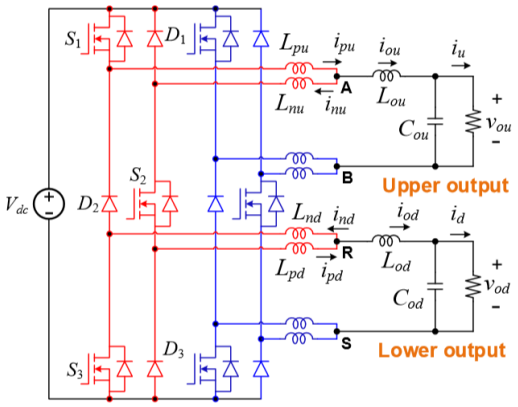

Figure 4 Single-phase six-switch dual-output inverter

Switching voltage	Switching modes								
	PP	ZZ	NN	PZ	PN	ZP	ZN	NP	NZ
V_u	0	0	0	V_{dc}	0	0	V_{dc}	$-V_{dc}$	$-V_{dc}$
V_d	0	0	0	V_{dc}	V_{dc}	$-V_{dc}$	0	$-V_{dc}$	0

5. DESIGN OF LIMITING INDUCTORS AND FILTER CIRCUIT DESIGN.

The limiting inductors L_p and L_n can be designed same as the three phase VSI filter inductor. This filter inductor equation is given by $L>\frac{0.03Vin}{2\pi f \Delta iLmax}$. where V_{in} is the DC input voltage, f is the fundamental frequency. Δi_{Lmax} is the maximum value of change in inductor current.

For Vin=12V, fundamental frequency(f) = 50Hz, ΔiLmax= 2.5A, L>458μH. L≈470μH. And filter capacitor is given by $C=\frac{1}{(L)(2\pi fc)^2}$,where $f_c<\frac{fsw}{10}$, fsw is the switching frequency. Calculating for C from above equation, C= 25μF. By using above equations inductor $L_n=L_p$=470μH the total inductance.

Two filter inductor L_f for upper and lower outputs. And the remaining inductances can serve as L_p and L_n. take Lf=150 μH and the remaining inductance is 160 μH. This 160 μH inductance is shared with eight inductors four for upper and four inductors for lower outputs. Therefore L_p= L_n=20 μH.

6. GATE DRIVE CIRCUIT

Carrier based PWM with offset technique is used for the gate drive circuit. By using the discontinuous PWM method for gate switching the switching losses can be reduced. This discontinuous PWM can be achieved by giving offset for the lower and upper references. Here the triangular wave is the carrier and reference are sinusoidal with some offset. Equations for the sine wave is given below.

v_{Au} =0.5+0.5$m_u$sin(2𝜋f_ut)

v_{Bu}=0.5+0.5$m_u$sin(2𝜋f_ut+𝜋)

v_{Rd}=0.5+0.5$m_u$sin(2𝜋f_ut)

v_{Sd}=0.5+0.5$m_u$sin(2𝜋f_ut+𝜋).

where, v_{Au}, v_{Bu} and v_{Rd}, v_{Sd} are the reference signal for upper terminals and lower terminals respectively.

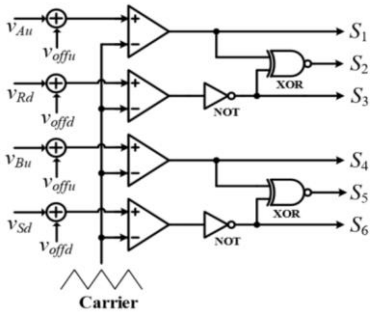

Figure 5 gate drive circuit for single-phase six-switch dual output inverter

COMPONENTS	RATINGS
INPUT VOLTAGE	12V DC
SWITCHING FREQUENCY	30kHz
LIMITING INDUCTORS	20 μH
FILTER INDUCTORS	150 μH
FILTER CAPACITOR	25 μF

The offset values are decided based on the fact that upper reference should always be larger or equal to lower reference. Based on this condition for the upper reference positive offset is added and for the lower reference negative offset is added. 1-max_u≥v_{offu}≥v_{offd}≥-min_d. Where, max_u=max(v_{Au}, v_{Bu}) and mind =min(v_{Rd}, v_{Sd}).

The value of v_{offmax}=1-max_u and v_{offmin}=1-min_d represent the maximum and minimum offsets, respectively.

7. SIMULATION AND IT'S RESULTS

Circuit is designed for input dc voltage of 12V switching frequency of 30kHz for the resistive load. Resistive load RL = 35 ohm. Modulation index used is m_u=0.6 and m_d=0.8. And it is designed to be the two outputs obtained will have the same frequency that is common frequency mode. In MATLAB Simulink the required components for the circuit can be easily drawn and circuit topology can be built. And the circuit built in the MATLAB is given in the fig 6.

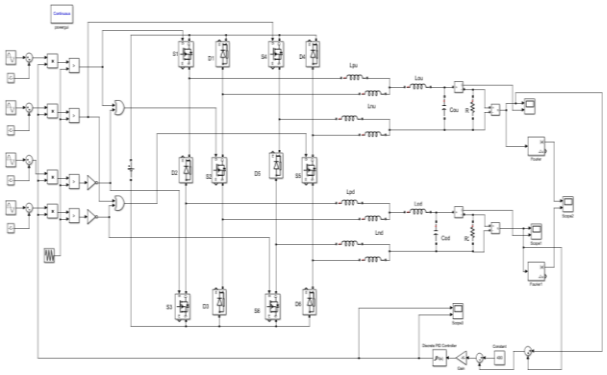

Figure 6 single-phase six-switch dual output inverter circuit built in MATLAB

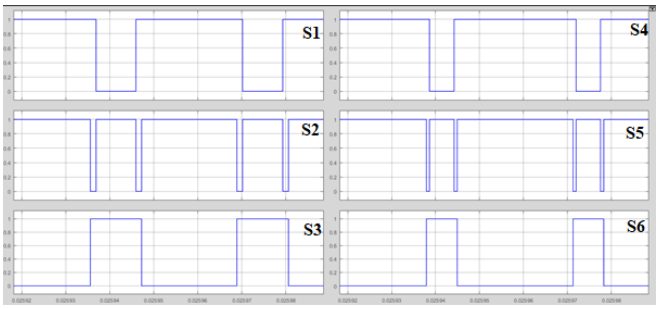

Figure 7 pulses generated for the switches for S_1, S_2, S_3, S_4, S_5, and S_6

PWM technique is used which produces the pulse as shown in the fig 7. The pulse generated for S_1, S_2, S_3, S_4, S_5, and S_6 and is given to the respective switches. After running the circuit, the voltage and current waveform for the two outputs upper and lower outputs are given in the figures 8 and 9 respectively. The magnitude of the output voltage for upper and lower output voltage are given by the fig 10. and the magnitude of the output voltage is 6.3VThe figure 11 shows the currents through the limiting inductors. i_{pu} and i_{nu} are the currents through inductors L_{pu} and L_{nu} respectively. The currents i_{nd} and i_{pd} are the currents through L_{nd} and L_{pd} respectively.

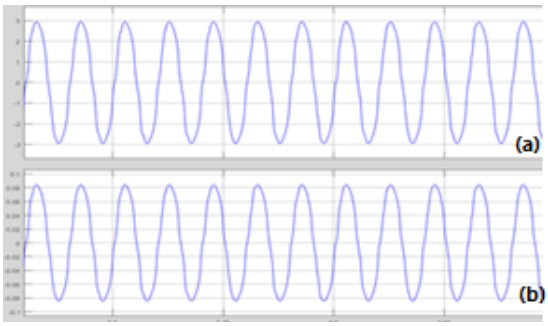

Figure 8 (a) (b) upper output voltage and current for resistive load

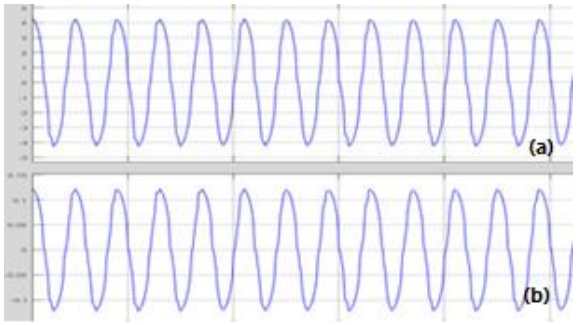

Figure 9 (a) (b) lower output voltage and current for resistive load

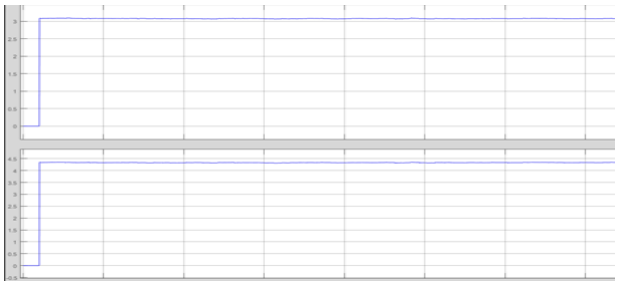

Figure 10 Magnitudes for upper and lower output

The frequency of the two outputs are ranging from 49.8Hz – 50.2Hz. The frequencies for the two outputs upper and lower are shown in the figure 12.

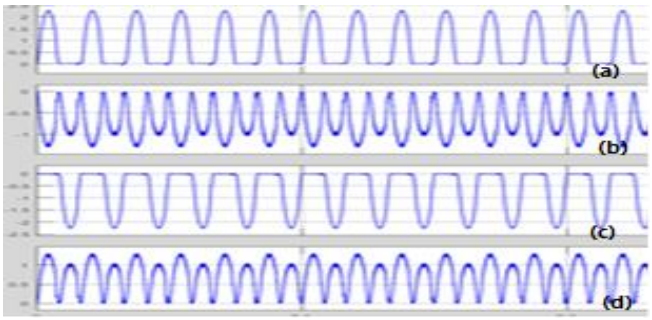

Figure 11 (a),(b),(c),(d) are the upper and lower limiting inductor currents i_{pu} and i_{nu}, i_{nd} and i_{pd}

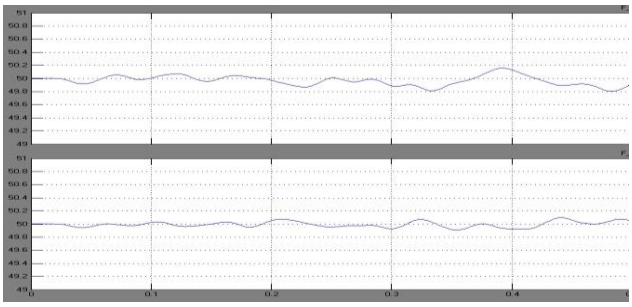

Figure 12 upper and lower output voltages having same frequency

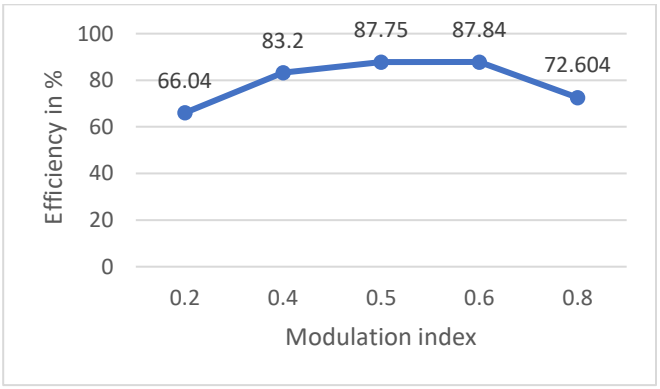

Figure 12 Graph (efficiency verses modulation index

Output voltages for different modulation index values are noted and efficiency for particular is calculated and this is shown in the above graph figure 12.

8. CONCLUSION

The proposed dual buck three-switch-leg structure is used for the implementation of single-phase six-switch dual output inverter. Compared to conventional this circuit uses less no of switches and thus power circuit for gate drive also reduced. The short circuit problem in conventional circuit is effectively eliminated due to the use of limiting inductors. Output are obtained for the input 12V DC. And the three-level output is obtained. The two outputs obtained in the dual output inverter is designed for common frequency. The proposed converter has high reliability. This circuit can be used for two low voltage AC applications at a time. Efficiency and results are good.

REFERENCES

[1] Bang Le-Huy Nguyen, Honnyong Cha, *IEEE*, and Heung-Geun Kim, *IEEE*- "Single-Phase Six-Switch Dual-Output Inverter Using Dual-Buck Structure."-IEEE 2017

[2] G. T. Kim and T. A. Lipo, "VSI-PWM rectifier/inverter system with a reduced switch count," IEEE *Trans. Ind. Appl*-1996.

[3] C. B. Jacobina, I. S. de Freitas, E. R. C. da Silva, A. M. N. Lima, and R. L. D. A. Ribeiro, "Reduced switch count dc-link ac_ac five-leg converter," *IEEE Trans. Power Electron.*, Sep. 2006.

[4] A. Fatemi, M. Azizi, M. Mohamadian, A. Y. Varjani, and M. Shahparasti, "Single-phase dual-output inverters with three-switch-legs," *IEEE Trans. Ind. Electron.*, May 2013.

[5] C. Liu, B. Wu, N. R. Zargari, D. Xu, and J. Wang, "A novel three-phase three-leg ac/ac converter using nine IGBTs", IEEE *Trans. Power Electron.*, May 2009.

[6] F. Gao, L. Zhang, D. Li, P. C. Loh, Y. Tang, and H. Gao, "Optimal pulse width modulation of nine-switch converter," IEEE *Trans. Power Electron.*, 2010.

[7] S. M. Dehghan, M. Mohamadian, A. Yazdian, and F. Ashrafzadeh, "A dual-input-dual-output Z-source inverter," *IEEE Trans. Power Electron.*, 2010.

[8] E. C. dos Santos, C. B. Jacobina, and O. I. da Silva, "Six-phase machine drive system with nine-switch converter," in *Proc. 2011 IEEE 37th Annu.* Nov. 2011.

[9] P. Sun, C. Liu, J. S. Lai, C. L. Chen, and N. Kees, "Three-phase dual-buck inverter with unified pulse width modulation," IEEE *Trans. Power Electron.*, Mar. 2012.